RESEARCH ARTICLE OPEN ACCESS

Implementation of Universal Asynchronous Receiver and Transmitter

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ABSTRACT
Universal Asynchronous Receiver Transmitter (UART) is the serial communication protocol that is used for data exchange between computer & peripherals. UART is a low velocity, short-distance, low-cost protocol. UART includes three modules which are received, the baud rate generator and transmitter. The UART design with Very High Description Language can be integrated into the Field Programmable Gate Array to achieve stable data transmission and to make system reliable and compact. In the result and simulation part, this project will focus on check the receive data with error free & baud rate generation at different frequencies. Before synthesizing of UART a baud rate generator is incorporated into the system. We use the frequency divider which sets itself to required frequency for the functionality at lower frequency. All modules are designed using VERILOG and implemented on Xilinx Suite development board.

I. INTRODUCTION

UART transmitter fetches a data word in parallel format and directing the UART to transmit it in a serial format. Likewise, the Receiver must detect transmission, which receive the data in serial format, and stores the data in a parallel format. As the UART is asynchronous in working, the receiver cannot acknowledge the incoming of data; receiver generates a local clock for the synchronisation of transmitter when start bit gets received. There is no need of generating separate clock by the transmitter. Transmitter and receiver agree timing parameters in advance for synchronizing the sending and receiving units.

UART is an integrated circuit which plays a predominant role in serial communication. ART acquires the function of conversion between the serial and parallel data. It provides Data Transfer between two systems is at great distance and there is reduction of signal distortion.

Parallel communication is a short distance communication with lot of multi bit address bus and data bus.

Serial communication is a long distance transmission communication and is widely used. But sometimes could not meet requirements due to Baud rate equipments. For low speed peripheral devices we use Serial communication. For complete communication FIFO Principle is used.

Why do we implement UART?

As UART can be used when there is no requirement for high speed and is inexpensive.

The protocol can be highly configurable. The major part is matching the serial bus baud rate.

Present Work

This project specifies and checks the receiver data with error free & baud rate generation at different frequencies.

Implementation of UART

The internal module of transmitter consists of parallel to serial converter and at the receiver end consists of serial to parallel converter.

In Asynchronous serial communication, sharing the clock with one another is not required, but the sender and receiver must agree timing parameters. Asynchronous transmission provides high reliability and long transmission distance. Hence, UART is used in data exchange between computer and peripherals.

UART allows full duplex communication in serial link. This paper uses Verilog HDL to implement the core functions of Serial communication.

UART communication needs only two signal lines (Rxd, Txd) for full duplex data communication.Txd is the transmit side which acts as output and Rxd is the receiver which acts as input. There are two states in the signal line, using logic 1(high) and logic 0 (low) to distinguish respectively.

Advantages

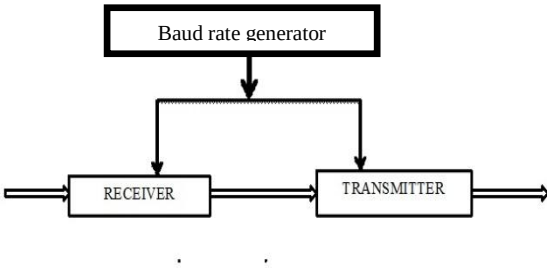
1. High bandwidth solution.
2. Line break and false start bit detection.
3. Reconfigurable.

II. BLOCK DIAGRAM

BAUD RATE GENERATOR

Baud Rate Generator is actually a frequency divider. The frequency clock produced by the baud

rate generator is not exactly the baud rate clock, but 16 times the baud rate clock. For sampling there exists the ideal time at the middle point of serial data bit.This output clock generated can be used as the receive reference clock by the receiver UART.



RECEIVER MODULE

During the UART reception, the serial data and the receiving clock are asynchronous, so it is very important to correctly determine the start bit of a frame data.

RXD transfers into logic 0 from logic 1which resembles as the beginning of a data frame. Once the start bit gets identified, next bit begin to count the rising edge of the baud clock, and when counting considers the sample RXD. Each value of the logic level gets placed in the register rbuf [7, 0] in order.

When the count equals 8, we can ensure that all the data bits are received, and are converted into a byte parallel data.

UARTs resynchronize the internal clocks on change of the data line. Due to resynchronisation they reliably receive when the transmitter is sending at a slightly different speed than it should. The other UARTs do not support this, and they resynchronize on the falling edge of the start bit only, and then read the center of each expected data bit, and this works if the broadcast data rate is accurate for allowance of the stop bits for reliability.Three error detection signals are commonly used in UART:

1. Parity Error used to justify the whether there exists even or parity by focussing on 1's.
2. Overrun Error specifies whether data is overwritten than expected.
3. A framing error occurs when the designated start and stop bits are not valid.

TRANSMITTER MODULE

The operationof transmit module is conversion of the sending 8-bit parallel data into serial data, adds start bit at the MSB of the data as well as the parity and stop bits at the LSB of the data. When the UART transmit module is reset, the transmit module immediately gets activated to send the data. The output appears as 1 start bit, 8 data bits, 1 parity bit and 1 stop bit. The parity bit is specified as the output. Finally, stop bit displays logic 1.

Depending on the manufacturer, specifies the different representations for UARTs Intel called their 8251 device as a "Programmable Communication Interface". The technique cannot send or receive data at high speed, but provides level of compatibility.

Importance of UART

1. Synchronisation Controls the reception and transmission time of the data
2. Increases the accuracy and reduces the effect of the noise

UART Functioning

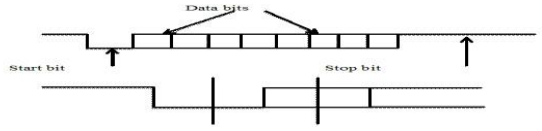
For the Full-duplex data communication UART needs only two signal lines (Rxd, Txd) to complete. Txd is the transmit side, which acts the output of UART; Rxd is the receiver, which is used as the input of UART. The two states in the signal line can be distinguished using logic 1 (high) and logic 0 (low).

The start bit is used for alerting the receiver that a word of data is about to be sent, and to force the clock in the receiver to get synchronized with the clock in the transmitter.

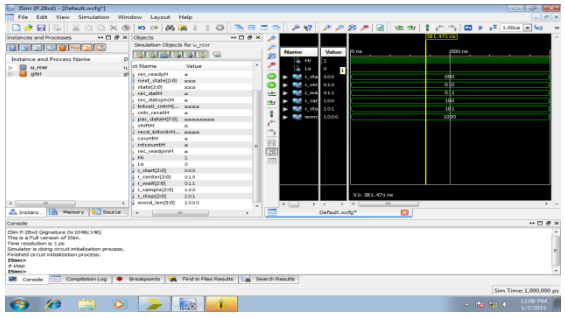
When the transmitter is idle state, the data line is in the logic high state. After the first bit, the individual bits are sent, with the least significant bit being sent first. Each bit in the transmission has to maintain exactly same amount of time and the receiver concentrates at approximately halfway for determining if bit is 0 or 1.The sender does not make sure when the receiver expected at the value of bit.

When the receiver receives all the bits of data word it concentrates on parity bit and then generates the stop bit. If the stop bit does not appear then it results in framing error. This is due to the variations in clocks of receiver and transmitter module.

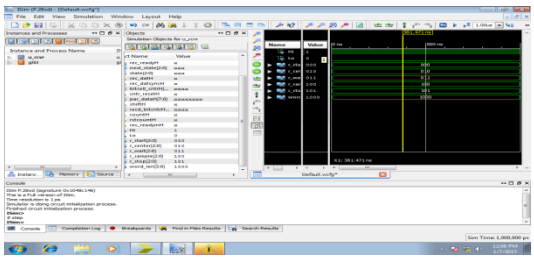
Irrespective of the received data the UART itself eliminates the start, parity and stop bits. If there is a new word ready for transmission the system gets self-synchronised. If there is no data to transmit, the transmission line can be idle.



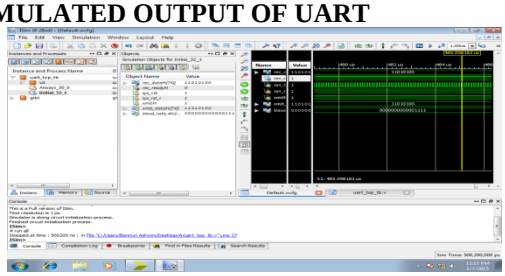
SIMULATED OUTPUT OF TRANSMITTER



SIMULATED OUTPUT OF RECEIVER



SIMULATED OUTPUT OF UART



III. CONCLUSION

In this paper, we proposed a design of UART with inbuilt Baud Rate generator. The design is successfully simulated using Xilinx ISE 14.2 suite software. The results are stable and reliable and show the correct functionality. Hence, we can improve the speed of UART by sending 16 bits per second of time. But by sending 16 bit ,it become more complex to count number of clock bit per unit time, so this can be overcome by using multichannel UART in future.

IV. FUTURE SCOPE

This can be implemented through hardware if an FPGA kit is available instead of software implementation. UART Channels can be increased to speed up the data transmission.

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